AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (Cancelled)

2. (Previously Presented) A method of synthesizing a register transfer level (RTL) based design of a system comprising the steps of:

determining a plurality of sub-modules of a top level system;

determining individual time budgets for each sub-module based on timing requirements of the top-level system;

synthesizing a gate-level design of said each sub-module based on the determined time budgets for said each sub-module;

testing the gate-level design of said each sub-module for conformance with design requirements of said each sub-module;

generating a netlist for said each sub-module when the gate level design of said each sub-module conforms to said design requirements of said each sub-module, then integrating the netlist of said each sub-module to form an integrated top level design netlist;

testing the integrated top-level design netlist for conformance with top-level design requirements; and

generating a top-level netlist when the integrated top-level design netlist conforms to the top-level design requirements.

Claims 3 - 4 (Cancelled)

5. (Previously Presented) A method of synthesizing a register transfer level (RTL) based design of a system comprising the steps of:

determining a plurality of sub-modules of a top level system;

determining individual time budgets for each sub-module based on timing requirements of the top-level system;

synthesizing a gate level design of - said each sub-module based on the determined time budgets for said each sub-module;

testing the gate level design of said each sub-module for conformance with design requirements of said each sub-module;

generating a netlist for said each sub-module when the gate level design of said each sub-module conforms to said design requirements of said each sub-module, then integrating the netlist of said each sub-module to form an integrated top level design netlist;

testing the integrated top-level design netlist for conformance with top-level design requirements; and

generating a top-level netlist when the integrated top-level design netlist conforms to the top-level design requirements,

wherein testing the gate level design of said each sub-module includes performing static timing analysis on said each sub-module for conformance with timing requirements for said each sub-module.

6. (Currently Amended) The method of claim 5, wherein the netlist is generated for said each ~~sub-modules~~ sub-module only if the timing requirements for said gate level design of said each sub-module are met.

7. (Previously Presented) The method of claim 6, wherein the step of synthesizing is re-performed and the gate level design of said each sub-module is re-tested in an iterative manner to verify conformance of the gate level design with the timing requirements of said each sub-module.

8. (Original) The method of claim 7, wherein the step of synthesizing is further based on wire loads and input/output loads/drivers.

9. (Currently Amended) The method of claim 8,~~on~~ wherein the step of testing the gate level design of said each sub-module for conformance with design requirements of said each sub-module includes performing a dynamic simulation on the gate level design of said each sub-module.

10. (Currently Amended) A method of synthesizing a register transfer level (RTL) based design of a system comprising the steps of:

determining sub-modules of a top level system;

determining individual time budgets for each sub-module based on timing requirements of the top-level system;

synthesizing a gate level design of said each sub-module based on the determined time budgets for said each sub-module;

generating a netlist for the gate level design of said each sub-module;

integrating the netlist of said each sub-module to form an integrated top level design netlist;

testing the integrated top-level design netlist for conformance with top-level design requirements; ~~and~~

generating a top-level netlist when the integrated top-level design netlist conforms to the top-level design requirements; and

testing the gate level design of said each sub-module for conformance with design requirements of said each sub-module prior to integrating the netlists to form the integrated top-level design netlist, wherein

testing the gate level design of said each sub-module includes performing static timing analysis on said each sub-module for conformance with timing requirements for said each sub-module, and

the netlist for the gate level design of said each sub-module is generated only if the timing requirements for said each sub-module are met.

Claim 11 – 14 (Cancelled)

15. (Currently Amended) The method of claim ~~14~~ 10, wherein the step of synthesizing is re-performed and the gate level design is re-tested in an iterative manner for verifying conformance of the gate level design with the timing requirements of said each sub-module.

16. (Previously Presented) The method of claim 15, wherein the step of synthesizing a gate level design is further based on wire loads and input/output loads/drivers.

17. (Previously Presented) The method of claim 16, wherein the step of testing the gate level design of said each sub-module for conformance with design requirements includes performing a dynamic simulation on the gate level design of said each sub-module.